

## 7th International Workshop on 2D Materials

**Title of the Presentation:** A native high- $\kappa$  gate dielectric for 2D electronics

**First Name:** Li

**Last Name:** Tianran

**Affiliation:** College of Chemistry and Molecular Engineering, Peking University, Beijing, China

**Email:** litr-cnc@pku.edu.cn



### Short Biography:

Tianran Li is a currently a PhD student in College of Chemistry, Peking University. He received his bachelor's degree in Peking University. His research mainly focuses on 2D semiconductors and 2D electronic devices.

### Abstract:

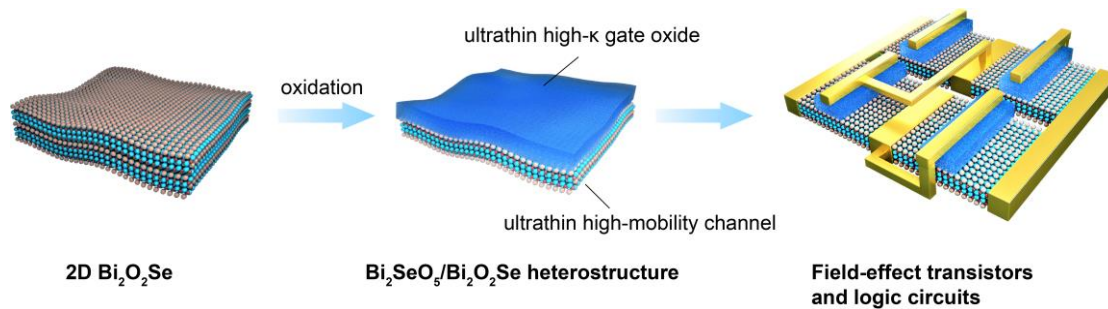


Figure.1 Fabrication of  $\text{Bi}_2\text{O}_2\text{Se}/\text{Bi}_2\text{SeO}_5$  field-effect transistors and logic circuits

The success of silicon as a dominant semiconductor in electronic industry largely owes to its native oxide counterpart, silicon dioxide. Synthesized simply by heating silicon wafer in oxygen atmosphere,  $\text{SiO}_2$  is highly dense, uniform and insulative and thus plays a very important role in all kinds of nanoelectronics devices. However, with the mainstream CMOS processing approaching sub-5 nm node, it became increasingly clear that Si/ $\text{SiO}_2$  system is coming to an end, as  $\text{SiO}_2$  has a far too low dielectric constant ( $\epsilon = 3.9$ ).

Recently, we found the native oxide of high-mobility two-dimensional  $\text{Bi}_2\text{O}_2\text{Se}$ ,  $\text{Bi}_2\text{SeO}_5$ , embodies both high interfacial quality and large dielectric constant. First-principle calculations showed that these two materials and form a typical type I heterojunction with band offset at both CBM and VBM larger than 1 eV, which is most suitable for field-effect devices. These transistors are fabricated with regional-selective etching and microfabrication techniques, showing carrier mobility  $> 300 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ ,  $I_{\text{on}}/I_{\text{off}} \sim 10^6$ , near-ideal subthreshold swing ( $SS < 75 \text{ mV/dec}$ ) as well as much reduced transfer curve hysteresis. Most importantly, effect oxide thickness (EOT) of these FETs can be as small as 0.9 nm, with gate leakage much smaller than thermal  $\text{SiO}_2$  of similar EOT. The inverter circuits constructed by these FETs have a maximum voltage gain  $>150$  at  $V_{\text{dd}} = 1 \text{ V}$ . Combined the ultra-thin planar structure of 2D materials and their natural resistance to short-channel effect, this material system can break through the bottleneck of modern electronic industry, and hopefully extend Moore's Law.

[1] Li, T. et al., *Nat. Electron.* 3, 473-478 (2020).

[2] Tu, T. et al., *Nano Lett.* 20, 7469-7475 (2020).