

7th International Workshop on 2D Materials

Title of the Presentation: Approaches to minimize operating voltages of MoTe₂ channel/P(VDF-TrFE) ferroelectric nonvolatile memory

First Name: Yongjae

Last Name: Cho

Affiliation: Department of Physics, Yonsei University, Seoul, South Korea

Email: dntmdgkfl@naver.com



Short Biography:

Yongjae CHO received the B.S. degree in physics from Yonsei University, Korea, in 2017, where he is currently pursuing the Ph.D. degree with the Institute of Physics and Applied Physics. The research area is doping of TMD based transistors.

Abstract: MoTe₂ channel-based P(VDF-TrFE) ferroelectric nonvolatile memory is fabricated, which operates at minimum switching pulse voltage and minimum drain voltage. For the minimum switching voltage of 8 V, bottom-gate architecture is employed and its advantages are investigated. By using bottom-gate structure, we could avoid a dead layer formed at the interface between thermally-deposited Al and P(VDF-TrFE) at top-gate architecture. A dead layer in top-gated ferroelectric memory transistors increases the coercive voltage so as the switching pulse voltage. And, for the minimum drain voltage, a novel method of H₂O₂ treatment is developed. By oxidizing the source/drain area of MoTe₂ surface by H₂O₂ solution, Ohmic contact between Pt and MoTe₂ is achieved even without thermal annealing which would have a destructive effect on the crystal quality of P(VDF-TrFE). To demonstrate the benefit of our memory transistor in aspect of power saving, it is integrated into an OLED operating circuit.

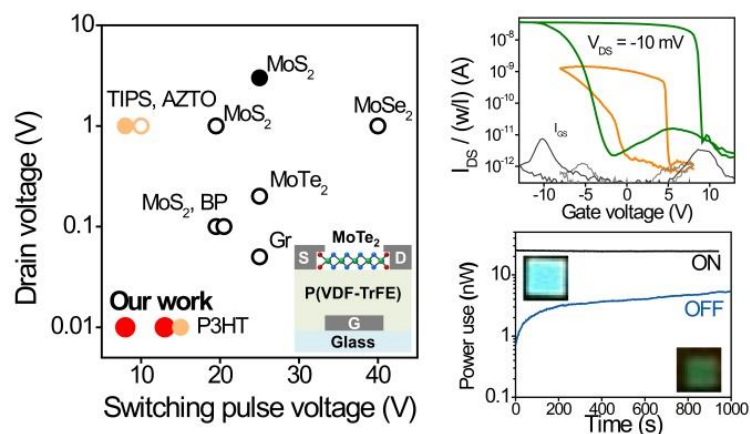


Fig. 1. Comparison plot showing switching pulse and drain/operation voltages of reported nonvolatile memory FETs, Memory hysteresis transfer and displacement characteristics, Power consumption-time plots of memory FETs